

INTRODUCTION

We face a dilemma in modern SoC design—power and performance considerations drive us towards larger collections of specialized hardware blocks, but time-to-market, design-cost and early software development considerations make this hard (or impossible) to achieve with current methodologies. Bluespectackles this problem by following the only possible way out of this dilemma, namely to dramatically raise the level of abstraction while maintaining quality synthesizability into silicon. Bluespec is rapidly being adopted by system architects and engineers at major design companies for exploration and design of the next generation chips.

FORMAT

The seminar will be run over three full working days. Each day will consist of three 90-minute lectures (two before and one after lunch), followed by an afternoon lab. Labs will consist of modifying and executing significant designs written using Bluespec. One of the labs will be targeted towards EVE's FPGA emulation platform. Teaching assistants who are Bluespec experts will be present.

FACULTY

Prof. Arvind (MIT Dept. of Electrical Engineering and Computer Science), a founder of Bluespec, Inc., and originator of its technology, will cover the key concepts with numerous motivating examples. The seminar is aimed at practicing engineers and faculty and advanced students in the area of ASIC and SoC design. At the end of the seminar, attendees should have a keen appreciation of these new technologies and how they may be applied immediately in their own future work.

WHO SHOULD ATTEND

This course is meant for engineers from Electrical and Computer Science Engineering. System architects to validation engineers will find the course very useful.

VENUE

To be finalised.

SCHEDULE

The course will be conducted during January 09 – 11, 2008, at IIT Bombay.

ACCOMMODATIION

Limited guest house facility in the campus is available for limited number of participants on payment as per the actuals and with advance request.

COURSE FEES

The course fee per participant is:

Industry	: Rs. 9,000/-
Academia (Faculty)	: Rs. 4,000/- (Affiliation Certificate required).

The fee includes course material, tea and working lunch during the coursedays.

REGISTRATION

Please fill out the attached Registration form and mail it along with the course fees to the course coordinator. Fees must be paid by a demand draft drawn in favour of “**Registrar, IIT Bombay (CEP A/c)**”.

Kindly note that no income tax is to be deducted at source from the course fee payments, as IIT Bombay is exempt from the same.

Please address all communication to:

Dr. Maryam Shojaei Baghini

(Course Coordinator)

Dept. of Electrical Engineering,

Indian Institute of Technology, Bombay

Powai, Mumbai - 400 076.

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Mobile : 9819869172

Fax : (022) 2572 3707

Email : mshojaei@ee.iitb.ac.in

PROGRAMME

Date	Handout	Topic	Time
Jan 9 th	Lec 1.1	Why Bluespec? (Context, some results on OFDM, H.264, Intel/IBM projects, SoC assembly and modeling; why not RTL/SystemC?)	9:00 - 10:30
	Lec 1.2	Intro to Rule & Synthesis (using GCD, binary multiplication example, how it maps into HW)	11:00-12:30
	Lec 1.3	Combinational Circuits & Synchronous Pipelines (using 802.11a & IFFT)	1:30-3:00
	Lab	Based on OFDM (4 th generation wireless modem)	3:15-5:00
Jan 10 th	Lec 2.1	Rules, Scheduling and Methods (Using IP lookup example; multiple architectures, turning rules into methods, compositionality of atomicity across modules)	9:00-10:30
	Lec 2.2	Modeling pipelined processor in Bluespec	11:00-12:30
	Lec 2.3	Interface abstraction: using caches as example (Get, Put, Client, Server, Cachelfc, mkConnecton, fifoToGet, fifoToPut,...)	1:30-3:00
	Lab	Processor Design	3:15-5:00
Jan 11 th	Lec 3.1	Issues in modern SoC design (components, composition, reuse, architectural exploration, software development, simulation speed, clocks and power management, mixed components)	9:00-10:30
	Lec 3.2	Designing an SoC using Bluespec (processors, interconnects and interconnect standards, DMAs, IP blocks)	11:00-12:30
	Lec 3.3	FPGA platforms for testing and SW development	1:30-3:00
	Lab	SoC integration	3:15-5:00

SHORT TERM COURSE ON

BLUESPEC – A New Way to Design SOCS and ASICS

January 09 – 11, 2008



APPLICATIONS MAY BE SENT SO AS TO REACH US NOT LATER THAN 9th
January 2008.

OFFICE OF
CONTINUING EDUCATION & QUALITY IMPROVEMENT PROGRAMMES

Indian Institute of Technology Bombay
Powai, Mumbai – 400 076.

REGISTRATION FORM

Short Term CEP Course on
BLUESPEC – A New Way to Design SOCS and ASICS

January 09 – 11, 2008

NAME (PRINT): _____ Gender: M / F

DESIGNATION: _____

ORGANIZATION: _____

MAILING ADDRESS: _____

TELEPHONE: _____ (O) _____ (R)

FAX: _____ MOBILE: _____

EMAIL: _____

QUALIFICATIONS: _____ EXPERIENCE: _____ Yrs.

IIT Guest House accommodation required?* YES / NO

PAYMENT: D.D.No.: _____ Dt _____ Rs _____

[Demand draft should be drawn in favour of "The Registrar, IIT Bombay (CEP A/c)"].

Date: _____ Signature of Applicant _____

***Guest House bill to be paid directly by participant.**

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